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# Correlation between stress-induced leakage current and dielectric degradation in ultra-porous SiOCH low-k materials

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Stress-Induced Leakage Current (SILC) behavior during the dielectric degradation of ultra-porous SiOCH low-k materials was investigated. Under high voltage stress, SILC increases to a critical value before final hard breakdown. This SILC increase rate is mainly driven by the injected charges and is negligibly influenced by temperature and voltage. SILC is found to be transient and shows a  $t^{-1}$  relaxation behavior, where  $t$  is the storage time at low voltages. This  $t^{-1}$  transient behavior, described by the tunneling front model, is caused by both electron charging of neutral defects in the dielectric close to the cathode interface and discharging of donor defects close to the anode interface. These defects have a uniform density distribution within the probed depth range, which is confirmed by the observed flat band voltage shift results collected during the low voltage storage. By applying an additional discharging step after the low voltage storage, the trap energies and spatial distributions are derived. In a highly degraded low-k dielectric, the majority of defects have a trap depth between 3.4 eV and 3.6 eV and a density level of  $1 \times 10^{18} \text{ eV}^{-1} \text{ cm}^{-3}$ . The relation between the defect density  $N$  and the total amount of the injected charges  $Q$  is measured to be sub-linear,  $N \sim Q^{0.45 \pm 0.07}$ . The physical nature of these stress-induced defects is suggested to be caused by the degradation of the Si-O based skeleton in the low-k dielectric. © 2015 AIP Publishing LLC.

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## I. INTRODUCTION

Low-k dielectric material plays an important role in advanced Back-End-of-Line (BEOL) technologies.<sup>1</sup> In highly scaled interconnect systems, signal delays largely increase due to reduced metal pitch and metal line thickness. Power consumption of the BEOL system is also an issue, as the chip working frequencies keep increasing. In order to overcome these challenges and maintain good system level performance, using ultra low-k dielectric materials in BEOL stacks is essential.<sup>2</sup> Replacing Si-O bonds with less polarized bonds and introducing porosity into the material are two effective approaches to achieve a lower dielectric constant than SiO<sub>2</sub>.<sup>3</sup> One example is porous SiOCH based low-k materials fabricated by Plasma Enhanced Chemical Vapor Deposition (PECVD). This type of low-k material provides k-values in the range between 3.0 and 2.0, depending on the porosity in the material.<sup>4,5</sup> Unfortunately, porous low-k dielectrics exhibit intrinsically weaker mechanical and electrical properties compared to SiO<sub>2</sub>. Also, integration processes degrade material robustness. Process induced material damage and modification are reported to be a major limitation for further k-value scaling.<sup>6,7</sup>

To achieve a reliable low-k integration, both intrinsic dielectric properties and integration process conditions need to be optimal. Such improvements strongly rely on fundamental material understanding.<sup>8</sup> One challenge is the

understanding of the complex structure of low-k materials caused by the nature of the PECVD technique and the use of co-deposition of matrix and porogen solutions.<sup>9</sup> Recently, it was shown that Stress Induced Leakage Current (SILC) can support this understanding. SILC is defined as the additional leakage current conducting through generated defects in the material under electrical stress.<sup>10</sup> SILC behavior varies in different low-k materials, as defect formation processes are highly dependent on the material structure.<sup>10,11</sup>

Moreover, SILC characteristics help to investigate dielectric degradation. In the field of low-k electrical reliability, one important issue is to correctly interpret Time Dependent Dielectric Breakdown (TDDB) parameters, such as the Weibull slope, the field acceleration, and the time to failure. From standard TDDB measurements, only limited information can be obtained, leading to a lot of discussions.<sup>12–15</sup> In literature, SILC monitoring is proven to be a powerful tool to study dielectric degradation in both thick and thin SiO<sub>2</sub> materials.<sup>10</sup> The analysis of SILCs during high field stress can be directly used to link the generated defect density with the dielectric degradation. The method of involving SILC measurements for understanding dielectric degradation has also been employed in the field of low-k dielectrics.<sup>16–18</sup> By investigating the effects of temperature and electric field on SILC, certain defect properties can be extracted.<sup>19,20</sup>

In this paper, we investigated SILC characteristics in an ultra-porous SiOCH low-k material (46% porosity). A theory was proposed to calculate the energies and the spatial distributions of the generated defects based on the experimental

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TABLE I. Detailed sample description.

Split	Type	Substrate	Dielectric	Metal barrier
S-1	MIS	n-Si	96 nm low-k	PVD TaN/Ta
S-2	MIM	n-Si + 10 nm TiN	95 nm low-k	PVD TaN/Ta
S-3	MIS	p-Si	89 nm low-k	PVD TaN/Ta
S-4	MIM	n-Si + 10 nm TiN	40 nm SiO <sub>2</sub>	PVD Ta
S-5	MIM	n-Si + 10 nm TiN	85 nm low-k <sup>a</sup>	PVD TaN/Ta

<sup>a</sup>After low-k deposition, the wafer, S-5, was exposed to the Xe capacitively coupled plasma discharge for 10 s with the direct contact to the plasma, i.e., no MgF<sub>2</sub> window (photon dose  $\sim 1.1 \times 10^{18}$  photons/cm<sup>2</sup>).

SILC results. In addition, the defect nature was discussed, as well as the relation between the defect density and the amount of injected charges.

## II. EXPERIMENTAL

### A. Tested samples

Dedicated metal-insulator-semiconductor (MIS) and metal-insulator-metal (MIM) planar capacitors with a SiOCH based ultra-porous low-k dielectric are fabricated. Detailed information of the test vehicle and the ultra-porous low-k dielectric can be found in Zhao *et al.*<sup>21</sup> and Urbanowicz *et al.*,<sup>22</sup> respectively. Table I lists detailed sample parameters, including dielectric thickness, metal barrier, and substrate type.

### B. Test procedures

#### 1. SILC measurement

As illustrated in Figs. 1(a) and 1(b), SILC measurements, using either a ramped voltage or a low constant voltage, are periodically performed during Constant Voltage Stress (CVS) measurements. Compared to the case for which a low constant voltage is applied, the use of a ramped voltage provides SILC

information within a wider voltage range and allows studying leakage mechanisms caused by the generated defects. The low constant voltage sense, on the other hand, ensures a more accurate SILC measurement at the selected voltage, due to less delay time between stress and sense.

#### 2. SILC relaxation measurement

The method to investigate SILC relaxation is shown in Fig. 1(c), where long term storages at a given low constant voltage are performed after CVS. A direct comparison between SILC relaxation measurements at different storage voltages is enabled by adding an additional sense step using a same sense voltage during these storages, as shown in Fig. 1(d). In addition, for MIS capacitors, Capacitance-Voltage (C-V) measurements can be performed during SILC relaxation measurements, as shown in Fig. 1(e). Fig. 1(f) illustrates our three-step test method consisting of a CVS stress, a SILC relaxation measurement and an extra 0 V storage.

## III. RESULTS AND DISCUSSION

### A. Typical SILC measurement

Fig. 2(a) shows SILC measurements using a ramped voltage on  $100 \times 100 \mu\text{m}^2$  capacitors from samples S-1 at 25 °C. The reference *I-V* curve obtained on a fresh capacitor shows an extremely low current in the voltage range below 50 V. While, in the same voltage range, the *I-V* characteristics of the device after being subjected to high voltage stresses show an increased current. This current, SILC, increases with increasing stress time. When a certain maximum damage in the low-k dielectric is reached, both the stress current  $I_{\text{stress}}$  and the SILC saturate. This current saturation has been discussed in our earlier work<sup>23</sup> and could be linked to different mechanisms.<sup>10</sup> In this paper, we limit our study to the SILC development before this saturation point. From Fig. 2(b), it can also be observed that the relative increase of SILC at different low voltages is the same in the semi-log *I-V* plot (parallel shift of the *I-V* curve with increasing stress time). Fig. 3 shows *I-V* results collected at 25 °C and 100 °C prior to CVS stress and at current saturation. It is shown that the SILC saturation level increases with temperature, while the increase rate of SILC with voltage remains exactly the same. The temperature independence of the *I-V* slopes suggest SILC to be a tunneling type current, which is unlike a Schottky emission (SE) or a Frenkel-Poole (FP) emission type of current, as both of them involve a temperature activation parameter in the leakage current slope,<sup>24</sup> which is not observed for our samples. Also, the extracted *k*-values based on SE or FP mechanisms are not realistic. Although tunneling currents are theoretically independent on temperature, we believe that the observed increase of the SILC saturation level is caused by the reported reduction in dielectric barrier height at high temperatures.<sup>25,26</sup>

Constant voltage sense results (Fig. 1(b)) are also obtained on  $100 \times 100 \mu\text{m}^2$  capacitors from samples S-1. Both the stress current  $I_{\text{stress}}$  and the sense current  $I_{\text{sense}}$  vs. stress time  $t_{\text{stress}}$  are measured at 25 °C and 100 °C and are plotted in Fig. 4. The maximum degradation at each stress

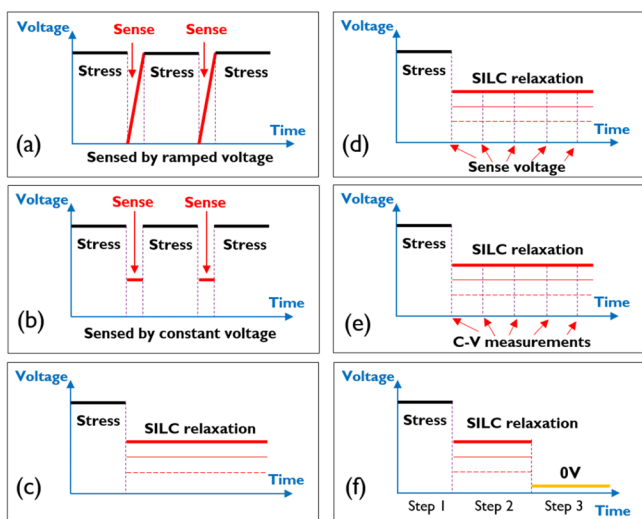


FIG. 1. (a) and (b) SILC measurements using a ramped voltage sense or a low voltage sense, respectively. (c) SILC relaxation test method. (d) and (e) SILC relaxation monitored by a sense voltage and C-V measurements, respectively. (f) Three-step measurement with an additional 0 V storage after SILC relaxation.

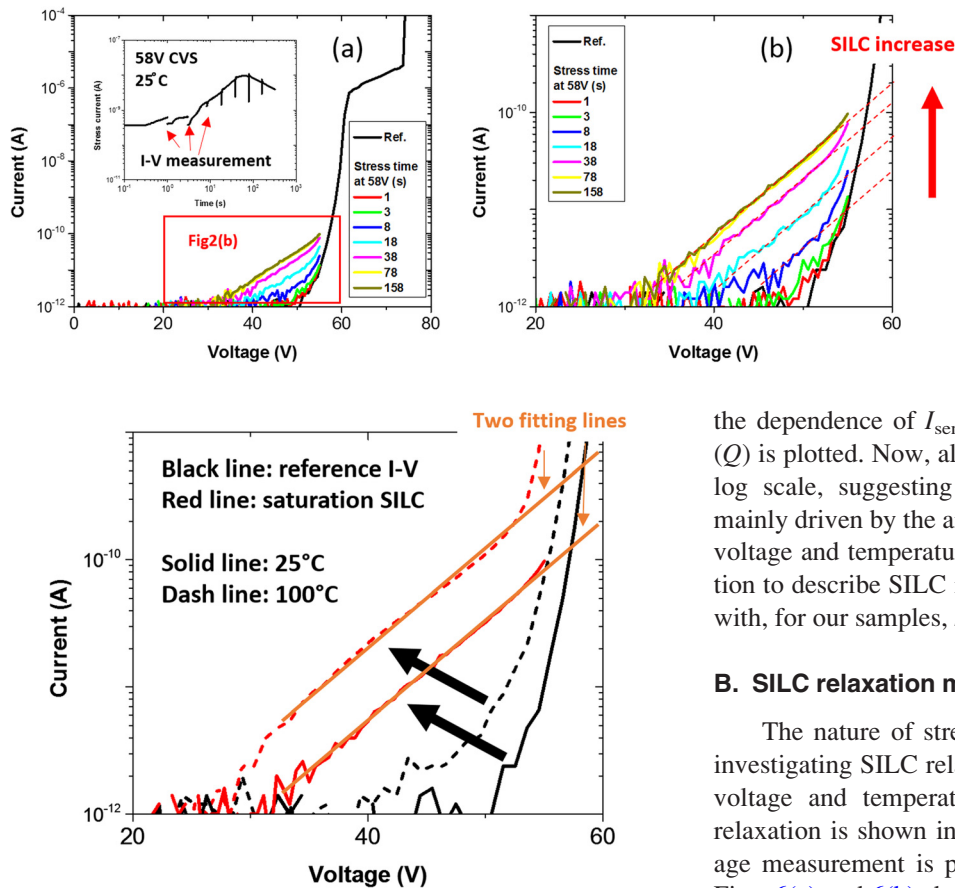


FIG. 3. Reference  $I$ - $V$  curve and SILC after reaching the saturation current collected both at 25 °C and 100 °C.

voltage results in the same  $I_{\text{sense}}$ , which shows that SILC indeed is proportional to dielectric degradation. Also, Fig. 4 suggests that both stress voltage and temperature seem to have a large impact on SILC increase. It should be noted that different stress voltages induce different amounts of damage for a given time and that different temperatures affect the slope of  $\log(I_{\text{sense}})$  vs.  $\log(t_{\text{stress}})$ . These are taken into account in our further analysis, as depicted in Fig. 5, where

the dependence of  $I_{\text{sense}}$  vs. the amount of injected charges ( $Q$ ) is plotted. Now, all graphs have a similar slope on a log-log scale, suggesting that the increased rate of SILC is mainly driven by the amount of injected charges, while stress voltage and temperature have a minor impact. A rough relation to describe SILC increase is suggested to be  $\text{SILC} \sim Q^m$  with, for our samples,  $m$  being 0.67.

## B. SILC relaxation measurement

The nature of stress-induced defects can be studied by investigating SILC relaxation ( $I_{\text{relax}}$ ) as a function of storage voltage and temperature. The method of studying SILC relaxation is shown in Fig. 1(c), where a low constant voltage measurement is performed for a long term after CVS. Figs. 6(a) and 6(b) show such measurement results collected at 25 °C and 100 °C on  $100 \times 100 \mu\text{m}^2$  capacitors from samples S-1. It can be observed that SILC is a fully transient current which disappears within 1000 s. These transient currents can be linearly fitted between  $\log(I_{\text{relax}})$  and  $\log(t_{\text{relax}})$  with a slope of  $-0.8$ . This slope-value remains the same for different stress levels and temperatures. The temperature insensitivity again indicates that the nature of SILC is a tunneling current. In Figs. 7(a) and 7(b), SILC relaxation measurements obtained at different storage voltages are shown at 25 °C and at 100 °C, respectively. Again, the same slope-value is observed. It should be noted from Figs. 6(b) and 7

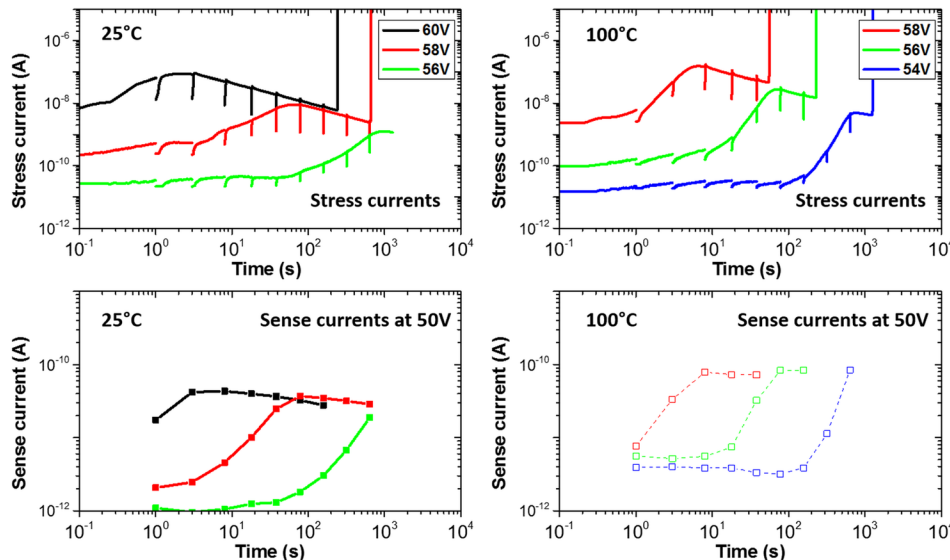


FIG. 4.  $I_{\text{stress}}$  and  $I_{\text{sense}}$  vs.  $t_{\text{stress}}$  measured at 25 °C and 100 °C.



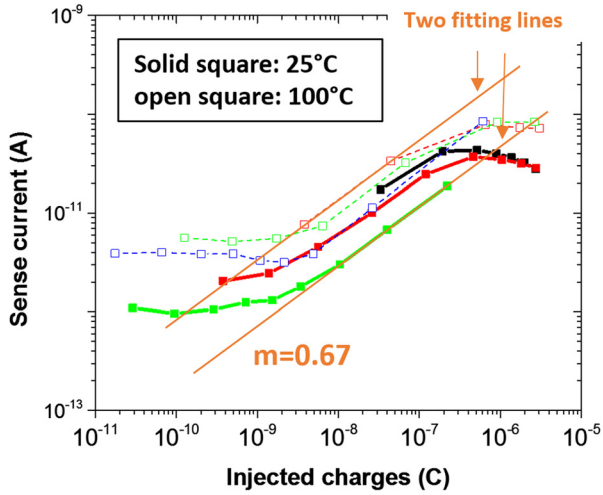


FIG. 5. SILC (or  $I_{\text{sense}}$ ) vs. the amount of injected charges calculated from the integration of  $I_{\text{stress}}$ . The colors of the curves represent the stress voltages as labelled in Fig. 4.

(b) that the 50 V storage at 100 °C causes additional dielectric degradation. Therefore, the experiments described in the remainder of this section are performed at 25 °C. To fully understand these SILCs, another measurement is designed, as shown in Fig. 1(d). The same sense voltage, 50 V, is applied during the storages at different low constant voltages. Only the higher storage voltage, 50 V, causes the “real” SILC relaxation, while the low storage voltages, 25 V and 0 V, only neutralize part of the SILC, as shown in Fig. 8.

### C. SILC theory: Tunneling front model

The transient SILC behavior measured in our SiOCH based ultra-porous low-k material strongly indicates electron charging of stress-induced neutral defects. The same  $I$ - $V$  slope of SILC and the same SILC relaxation behavior at low and high temperatures suggest these SILCs to be tunneling type currents. Finally, the observed slope-value of  $-0.8$  between  $\log(I_{\text{relax}})$  and  $\log(t_{\text{relax}})$  suggests a similar mechanism as the tunneling front model reported in SiO<sub>2</sub>. In earlier literature, it was found that electrons from the Si valence band are involved in the neutralization of holes trapped close to the Si substrate in SiO<sub>2</sub> by tunneling/recombination processes.<sup>27</sup> According to this theory, at a given time  $t_{\text{relax}}$ , traps within  $x(t_{\text{relax}})$ , the distance from Si/SiO<sub>2</sub> interface, are annealed out, while traps beyond  $x(t)$  are still empty. This  $x(t_{\text{relax}})$  can be calculated as

$$x(t_{\text{relax}}) = \frac{1}{2\beta} \ln\left(\frac{t_{\text{relax}}}{t_0}\right), \quad (1)$$

where  $\beta$  and  $t_0$  are tunneling parameters. In later studies,<sup>28</sup> this relation is proven to be able to describe electron charging of neutral defects generated by high field stresses in SiO<sub>2</sub>. The SILC relaxation,  $I(t_{\text{relax}})$ , due to electron charging, derived from Eq. (1), is then given by<sup>29</sup>

$$\begin{aligned} I(t_{\text{relax}}) &= A \cdot qnv = A \cdot qN(x(t_{\text{relax}})) \frac{dx}{dt} \\ &= A \cdot qN(x(t_{\text{relax}})) \cdot \frac{1}{2\beta t_{\text{relax}}}, \end{aligned} \quad (2)$$

where  $A$  is the capacitor area,  $q$  is the elementary charge,  $n$  is the carrier density,  $v$  is the front velocity, and  $N(x(t_{\text{relax}}))$  is the defect spatial distribution. It is clear from this equation that if the spatial distribution of generated defects is uniform within the probed depth range in the material,  $I(t_{\text{relax}})$  will be proportional to  $1/t_{\text{relax}}$ , resulting in a linear relationship between  $\log(I(t_{\text{relax}}))$  and  $\log(t_{\text{relax}})$  with a slope-value of  $-1$ . The slope-value,  $-0.8$ , measured in our work is very close to this theoretical value suggesting a uniform defect spatial distribution in the degraded low-k material.

To support this conclusion, flat band voltage ( $V_{\text{FB}}$ ) shifts during the SILC relaxation on stressed (60 s at 58 V, 25 °C)  $100 \times 100 \mu\text{m}^2$  capacitors from samples S-1 are measured at 25 °C. Fig. 9 shows  $\Delta V_{\text{FB}}(t_{\text{relax}})/|\Delta V_{\text{FB}}(0)|$  vs.  $t_{\text{relax}}$  at different low voltages.  $\Delta V_{\text{FB}}(0)$  after CVS stress is negative and  $V_{\text{FB}}$  is shifting in a positive direction during storage.  $\Delta V_{\text{FB}}(t_{\text{relax}})/|\Delta V_{\text{FB}}(0)|$  vs.  $\log(t_{\text{relax}})$  yields a linear relation. The same slope for samples that were stored at voltages between 0 V and 20 V is observed. This observation is reported to be the slow process of physical removal of donor type interface states,<sup>20</sup> which is independent of storage voltage. The increasing slope with increasing storage voltage above 20 V during SILC relaxation is due to additional electron charging in the system. Higher storage voltages introduce faster  $V_{\text{FB}}$  shifts, suggesting more trapped electrons. The linear relation between  $\Delta V_{\text{FB}}(t_{\text{relax}})/|\Delta V_{\text{FB}}(0)|$  vs.  $\log(t_{\text{relax}})$  can be derived by the calculation of accumulated charges,  $\Delta Q$ .  $\Delta Q(t_{\text{relax}})$  at a given relaxation time,  $t_{\text{relax}}$ , is expressed as<sup>30</sup>

$$\Delta Q(t_{\text{relax}}) = A \cdot q \int_0^{x(t_{\text{relax}})} N(x(t_{\text{relax}})) \cdot dx. \quad (3)$$

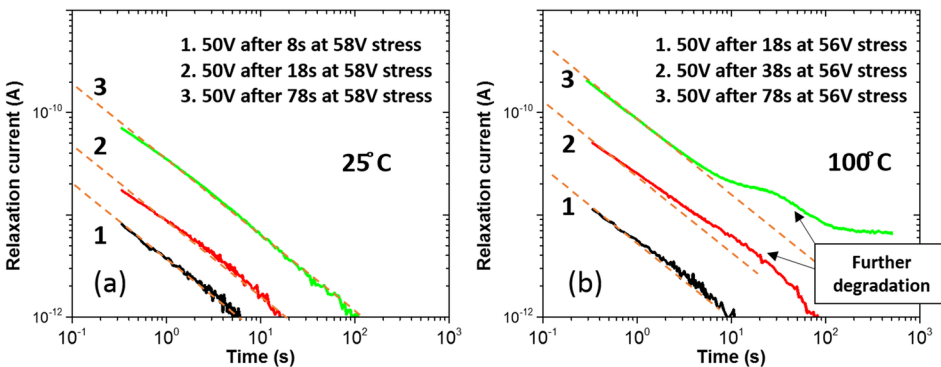


FIG. 6. (a) and (b) SILC relaxation measured using the same low voltage for the devices that already have been subjected to different amounts of high voltage stress at 25 °C and 100 °C, respectively. The relaxation current is the difference between the measured current in the degraded device and the initial leakage current in a fresh device, both obtained at 50 V.

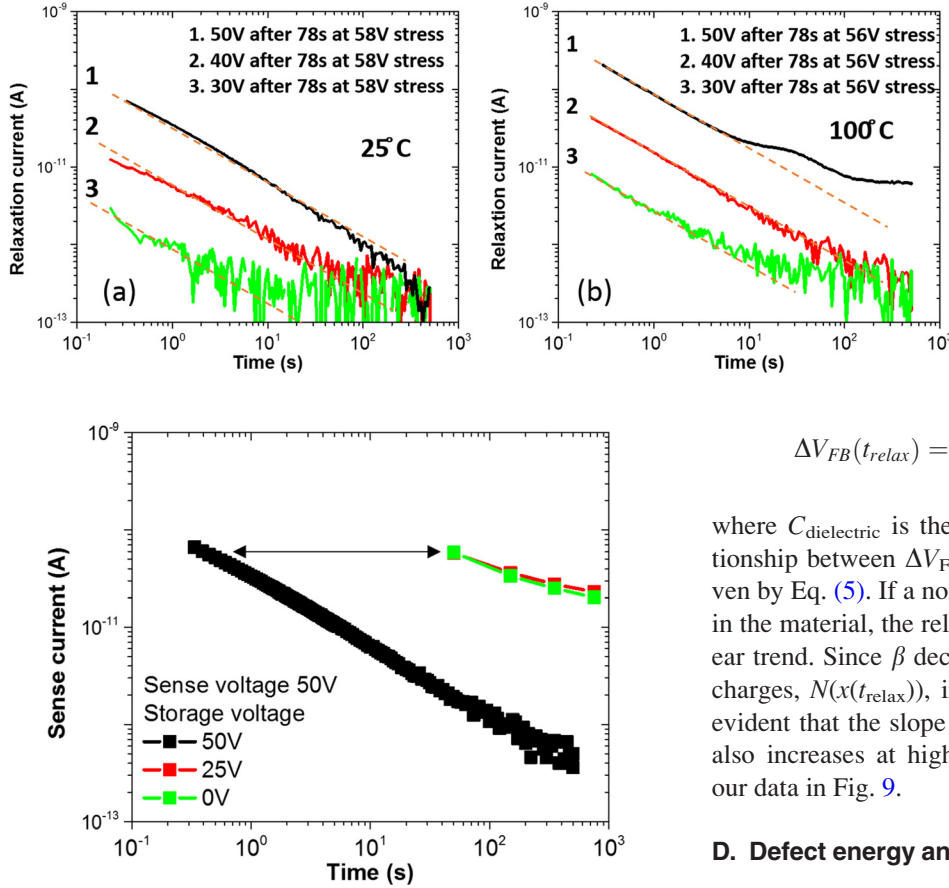


FIG. 8. SILC relaxation measured by the same sense voltage, 50 V, where the relaxation itself is done at different low storage voltages, 50 V, 25 V, 0 V at 25 °C.

Assuming a uniform defect distribution, Eq. (3) can be combined with Eq. (1) and lead to

$$\Delta Q(t_{\text{relax}}) = \frac{qN(x(t_{\text{relax}}))}{2\beta} \ln\left(\frac{t}{t_0}\right). \quad (4)$$

Finally, assuming a thick dielectric,  $\Delta V_{\text{FB}}(t_{\text{relax}})$  can be estimated as

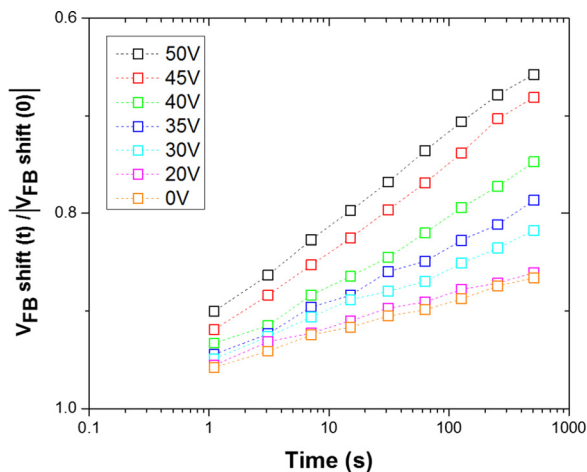


FIG. 9.  $\Delta V_{\text{FB}}(t_{\text{relax}})/|\Delta V_{\text{FB}}(0)|$  vs.  $t_{\text{relax}}$  during SILC relaxation measurements at different storage voltages.

FIG. 7. (a) and (b) SILC relaxation measured using different low voltages for the devices that already have been subjected to a certain level of high voltage stress at 25 °C and 100 °C, respectively. The relaxation current is calculated in the same way as described in Fig. 6.

$$\Delta V_{\text{FB}}(t_{\text{relax}}) = \Delta V(0) + \frac{qN(x(t_{\text{relax}}))}{2\beta \cdot C_{\text{dielectric}}} \ln\left(\frac{t}{t_0}\right), \quad (5)$$

where  $C_{\text{dielectric}}$  is the dielectric capacitance. A linear relationship between  $\Delta V_{\text{FB}}(t_{\text{relax}})/|\Delta V_{\text{FB}}(0)|$  vs.  $\log(t_{\text{relax}})$  is proven by Eq. (5). If a non-uniform defect distribution is present in the material, the relation in Eq. (5) will deviate from a linear trend. Since  $\beta$  decreases and the amount of total trapped charges,  $N(x(t_{\text{relax}}))$ , increases with increasing voltage, it is evident that the slope of  $\Delta V_{\text{FB}}(t_{\text{relax}})/|\Delta V_{\text{FB}}(0)|$  vs.  $\log(t_{\text{relax}})$  also increases at higher voltages, which is consistent with our data in Fig. 9.

#### D. Defect energy and spatial distribution

To investigate stress-induced defect energies and spatial distributions, a three-step measurement is designed, as shown in Fig. 1(f). In addition to the stress-relaxation method proposed in Fig. 1(c), a third step consisting of a storage at 0 V is added. A proposed physical model, which is initially applied to reliability studies on  $\text{SiO}_2$ ,<sup>31</sup> is illustrated in Fig. 10. In the second step, electrons are injected from the cathode into the low-k dielectric. The trap depth ( $E_t$ ) from the conduction band of low-k dielectric can be calculated as

$$E_t = (\phi - qxV/d), \quad (6)$$

where  $\phi$  is the barrier height of low-k material,  $x$  is the distance between the trap location and the electron injecting interface,  $V$  is the applied voltage, and  $d$  is the dielectric thickness. In the third step, the trapped electrons in the second step are discharged from the filled defects, resulting in a reversed current. At a given time ( $t_{\text{dis}}$ ), the position of the discharged defect,  $x_{\text{dis}}$ , can be calculated by Eq. (1). Using a more detailed format of  $\beta$  at 0 V, we have

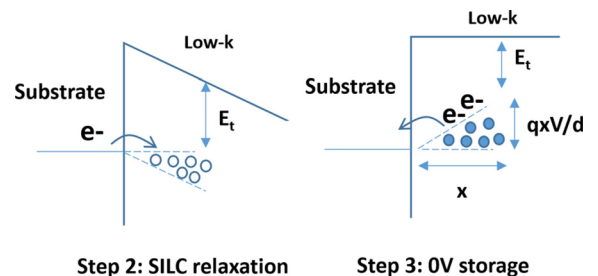


FIG. 10. Schematic of proposed charging/discharging theory.

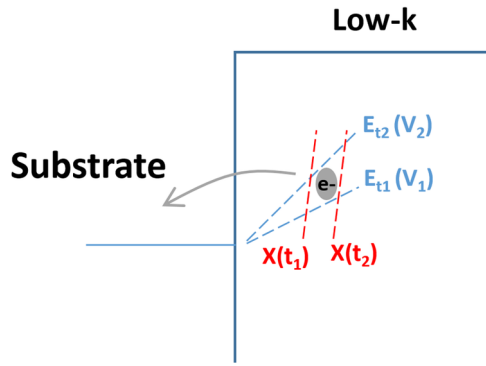


FIG. 11. The proposed method to determine the energies and the spatial distributions of the generated defects.

$$x_{dis} = \frac{\hbar}{2\sqrt{2m^*E_t(x_{dis})}} \ln\left(\frac{t_{dis}}{t_0}\right), \quad (7)$$

where  $\hbar$  is the reduced Planck constant,  $m^*$  is the tunneling effective mass, and  $E_t(x_{dis})$  is the trap depth at  $x_{dis}$ .  $E_t(x_{dis})$  can be calculated based on Eq. (6) using the applied charging voltage in the second step. Therefore, as shown in Fig. 11, the amount of charges,  $Q$ , in between locations:  $x(t_{dis\_1})$  and  $x(t_{dis\_2})$ , and trap depths:  $E_t(V_{charg\_1})$  and  $E_t(V_{charg\_2})$  can be calculated by integrating the difference between the discharging currents,  $I_{dis}$ , measured in the third step as

$$Q = \int_{t_{dis1}}^{t_{dis2}} (I_{dis}(V_{charg1}) - I_{dis}(V_{charg2})) \cdot dt. \quad (8)$$

For four degraded  $1000 \times 1000 \mu\text{m}^2$  capacitors from samples S-1 measured at  $25^\circ\text{C}$ , the results collected at the second and third steps are shown in Figs. 12(a) and 12(b). During SILC relaxation, step two, voltages of 50 V, 40 V, 30 V and 20 V are applied and plotted with thick lines in Fig. 12(a). The discharging currents during step 3 are observed to be negative. The absolute value of these currents is then plotted in Fig. 12(a) using thin lines. It can be seen from this figure that the discharging currents in step 3 have the same slopes compared to the currents obtained during SILC relaxation in step 2 when using log-log scale plotting, which validates the format of Eq. (2). The zoom-in of the discharging current in step 3 is shown in Fig. 12(b). A higher charging voltage used during SILC relaxation causes higher discharging currents, confirming the principle of the proposed theory. Fig. 13

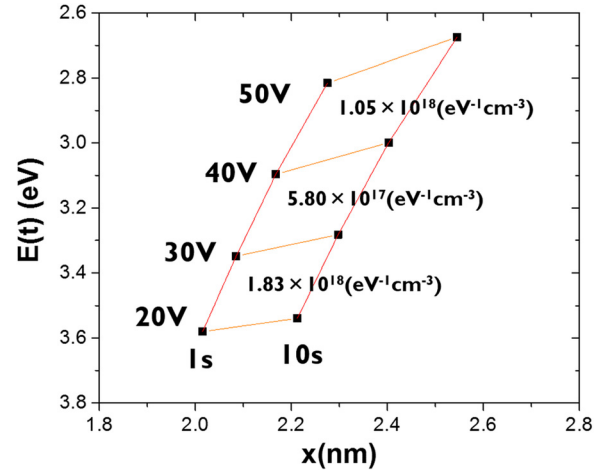


FIG. 13. Defect energies and spatial distributions in the degraded low-k dielectric.

summarizes the defect energies and spatial distributions based on the calculation of  $I_{dis}(50 \text{ V})$ ,  $I_{dis}(40 \text{ V})$ ,  $I_{dis}(30 \text{ V})$ , and  $I_{dis}(20 \text{ V})$  within the time window of 1 s–10 s. The parameters used in Eqs. (6)–(8) are listed in Table II. The maximum trap density in the stressed low-k dielectric is found to be close to the Si conduction band with a trap depth range of 3.4 eV–3.6 eV and in the order of  $1 \times 10^{18} \text{ eV}^{-1} \text{ cm}^{-3}$ , which is slightly higher than the one reported in the stressed thermal oxide.<sup>32</sup>

## E. Relation between defect density and injected charges

In order to further explore the relation between degradation level and generated defects, we again use  $1000 \times 1000 \mu\text{m}^2$  capacitors from sample S-1 at  $25^\circ\text{C}$ . These devices are first stressed to four different levels, as shown in Fig. 14(a). Then, a low voltage of 40 V is applied on these stressed devices.  $I_{sense}$  recorded after 1 s storage at 40 V is plotted versus the amount of injected charges ( $Q$ ) during stress in Fig. 14(b), which shows a similar trend compared to the one in Fig. 5. The long term relaxation currents at 40 V storage are shown in Fig. 15(a) with thick lines. After that, 0 V is applied on these devices to monitor discharging currents. The absolute values of these discharging currents are also plotted in Fig. 15(a) with thin lines. The average defect density ( $N$ ) that can be charged by 40 V is equal to the total amount of

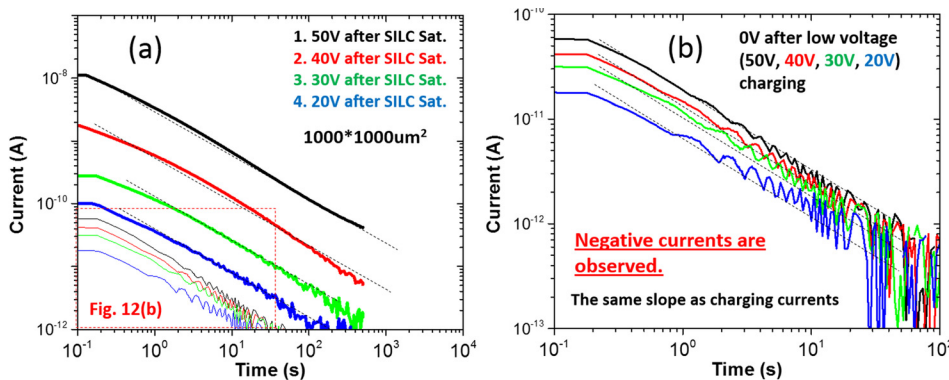


FIG. 12. (a) Thick lines: charging currents during SILC relaxation using different low voltages for the devices already subjected to the same level of high voltage stress (Step 2 in Fig. 1(f)). Thin lines: discharging currents (absolute value) in the 0 V discharging step (Step 3 in Fig. 1(f)). (b) Zoom in of the low current region shown in Fig. 12(a).

TABLE II. The parameters in Eqs. (6)–(8) used for Fig. 13.

Parameter	Value	Unit
Reduced Planck constant	$1.05 \times 10^{-34}$	J s
Elementary charge	$1.60 \times 10^{-19}$	C
Tunneling effective mass ( $0.42m_0$ ) [from Ref. 27]	$3.83 \times 10^{-31}$	Kg
$t_0$ [from Ref. 31]	$1 \times 10^{-11}$	s
Low-k barrier height [from Ref. 23]	4.0	eV

discharging electrons in step 3, which is calculated by integrating  $I_{\text{dis}}$  over time. Fig. 15(b) shows the relationship between normalized  $N$  vs.  $Q$ . A sub-linear relationship,  $N \sim Q^{0.45 \pm 0.07}$ , is estimated from Fig. 15(b) and is different from the previously reported linear relationship between  $N$  vs.  $Q$  in low-k degradation theories.<sup>12,33</sup> In addition, the relation between SILC ( $I_{\text{sense}}$ ) and  $N$  can be also calculated as  $\text{SILC} \sim N^{1.48}$ .

Capacitors with the same size from MIM samples S-2 are tested using the same procedure and  $I_{\text{sense}}$  vs.  $Q$  and  $N$  vs.  $Q$  are added in Figs. 14(b) and 15(b), respectively, where the  $I_{\text{sense}}$  and  $N$  values are normalized in order to fit the data obtained on the MIS samples S-1. As  $I_{\text{sense}}$  and  $N$  are all plotted with  $Q$  in a log-log scale, these normalizations do not change the observed increasing trends. Similar relations of  $I_{\text{sense}}$  vs.  $Q$  and  $N$  vs.  $Q$  in the samples S-2 are obtained, suggesting that no difference exists between measurements using MIS and MIM configurations. These results exclude the possible influences from the transition interface between the Si substrate and the low-k dielectric. Therefore, it is confirmed that the mechanism discussed in this paper is caused by the low-k material degradation.

## F. Additional SILC characterization

In previous sub-sessions, only the interface between the Si substrate and the low-k material was studied. We found that close to this interface, neutral defects are generated inside the low-k material during CVS stress causing electron charging at low voltages and discharging at 0 V, as depicted in Fig. 10. However, in all SILC relaxation measurements discussed above, the currents measured from two electrodes are identical, which could imply that during the charging step, electron discharging also occurs at donor type defects close to the metal/low-k interface. As illustrated in Fig. 16, electrons could flow into barrier metal and leave positively charged defects in the low-k dielectric.

This is further elaborated by our measurements of  $100 \times 100 \mu\text{m}^2$  capacitors from the p-type substrate sample S-3 at 25 °C. By applying a negative bias to the metal electrode, the electron injection is changing from the Si substrate/low-k interface to the metal/low-k interface, while the anode is changing from the barrier metal to the Si substrate. As a consequence, when applying a low negative voltage after a high negative CVS stress, electrons charge the neutral defects at the metal/low-k interface and discharge from the donor defects at the Si substrate/low-k interface. As shown in Fig. 17(a), the combination of using both negatively biased stress and SILC relaxation in our S-3 devices shows the same transient relaxation behavior,  $t^{-1}$ , compared to the case where a positive bias stress and SILC relaxation was performed on the sample S-1 discussed in Fig. 6(a). These results suggest that the degradation mechanism in the studied low-k dielectric is interface independent. Moreover, the combination of using a negative bias stress and a positive

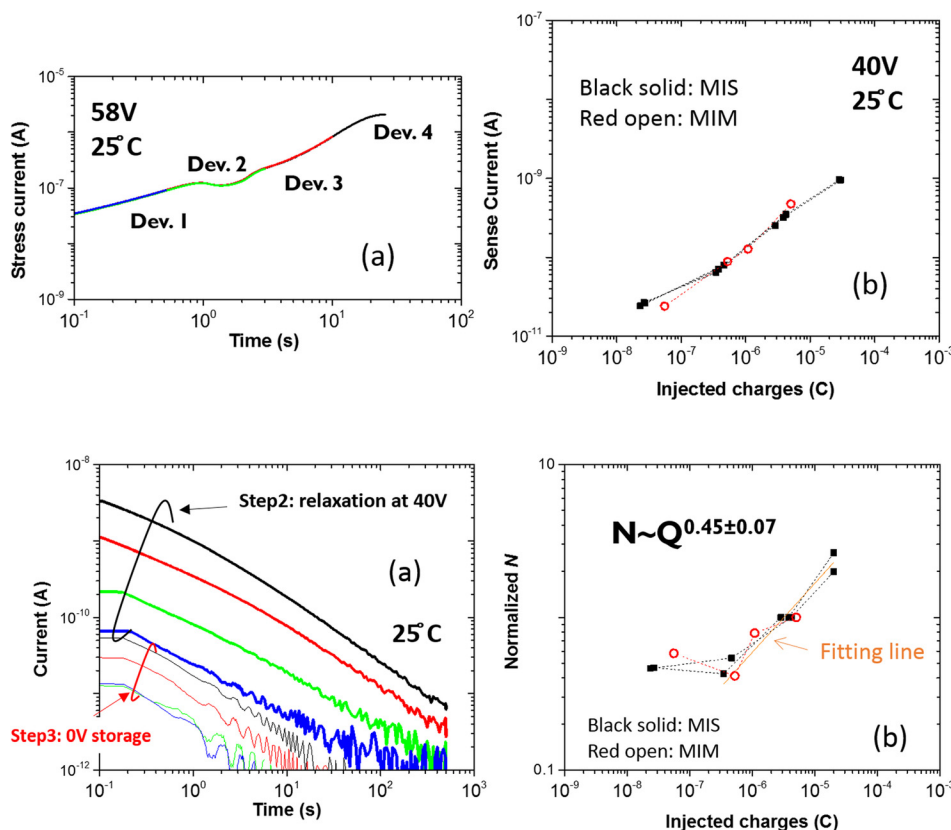


FIG. 14. (a)  $I_{\text{stress}}-t_{\text{stress}}$  relations at different stress levels. (b)  $I_{\text{sense}}$  measured at 40 V vs. the amount of charges injected during stress.

FIG. 15. (a) Thick lines: SILCs measured using the same low voltage for the devices already subjected to different levels of high voltage stress. Thin line: discharging currents (absolute value) in the 0 V discharging step. (b) Relation between the relative increase in the average defect density ( $N$ ) vs. injected charges ( $Q$ ).



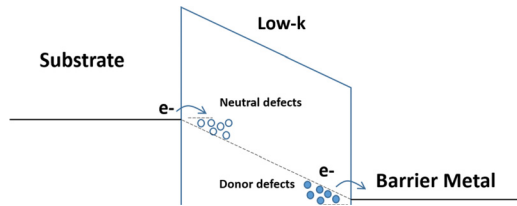


FIG. 16. Schematic of the charging process at the substrate/low-k interface and the discharging process at the metal/low-k interface.

bias SILC relaxation obtained on our S-3 devices shows a similar SILC relaxation trend with an opposite direction, as shown in Fig. 17(a), indicating that at the Si substrate/low-k interface, both donor and neutral defects with a similar defect density are generated by the high voltage stress. As illustrated in Fig. 17(b), at the Si substrate/low-k interface, a negative bias SILC relaxation step leads to donor defect discharging, while a positive bias SILC relaxation step leads to electron charging of neutral defects. We also collected capacitance-voltage (*C-V*) curves after applying positive, negative, and zero voltage during the SILC relaxation step on our S-3 devices. In Fig. 18, these *C-V* curves are compared with the curves measured from both a fresh sample and a sample after being subjected to high negative CVS stress. SILC relaxation at 0 V only causes a small relaxation towards the positive direction. The positive bias SILC relaxation, on the other hand, causes a larger *C-V* curve shift towards the positive direction. Finally, the negative bias SILC relaxation causes a *C-V* curve shift towards the negative direction. In addition, no measurable current was detected during 0 V SILC relaxation. These results are in a good agreement with the proposed mechanism in Fig. 17(b).

### G. Discussion of the nature of defects causing SILC

The SILC characteristics discussed in this work share a lot of similarities to the results reported for SiO<sub>2</sub>. First, the relative increase of SILC is mainly driven by injected charges.<sup>10</sup> Second, neutral defects, as well as donor type defects, are generated symmetrically in the degraded dielectric with a uniform defect density close to both the cathode and the anode interfaces.<sup>34</sup> Third, the charging and discharging currents show a  $t^{-1}$  relation and can be explained by the

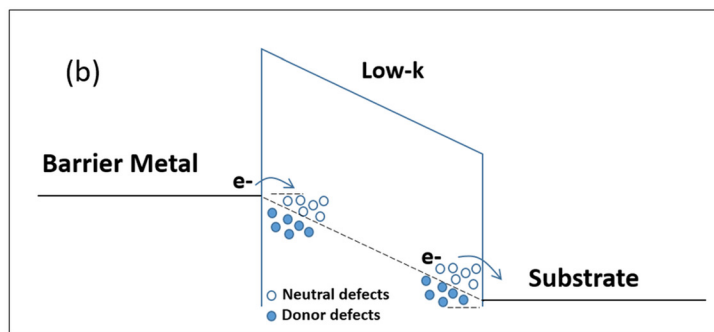
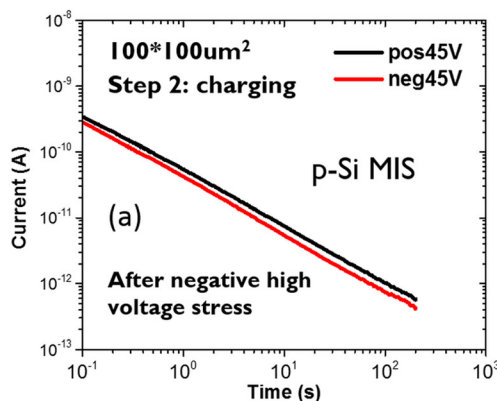


FIG. 17. (a) SILC relaxation measured using the same low voltage with both positive and negative voltages measured on devices that have been already subjected to the same amount of high negative voltage stress. (b) Schematic of proposed charging/discharging theory.

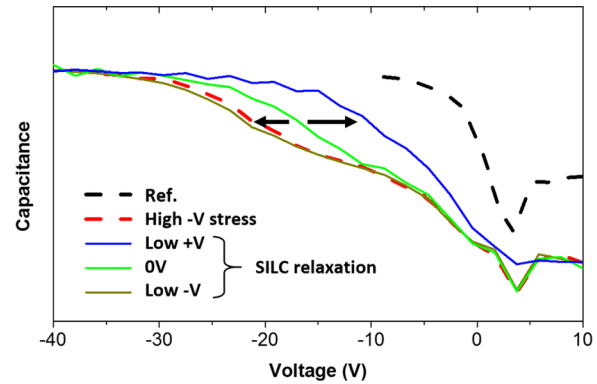


FIG. 18. Capacitance-voltage (*C-V*) curves collected after applying positive, negative, and zero voltage during the SILC relaxation obtained on our S-3 devices. The curves measured from both a fresh sample and a sample after being subjected to high negative CVS stress are also plotted in the same figure.

tunneling front model. It was shown that the transient currents normally occur in thick SiO<sub>2</sub> (>8 nm) and become constant SILCs in thin SiO<sub>2</sub> (<5 nm).<sup>35</sup> Our data show that this transient SILC behavior can be also observed in 40 nm SiO<sub>2</sub>. As shown in Fig. 19, *I-V* measurements on three 100 × 100 μm<sup>2</sup> MIM capacitors with 40 nm SiO<sub>2</sub> are performed at 100 °C for (a) fresh device, (b) high voltage stressed device, and (c) low voltage stored device after high voltage stress. It can be found that the SILC is generated in the low voltage range after CVS stress, but it completely disappears after an additional low voltage storage. The SILC relaxation results in a  $t^{-0.9}$  relation, as shown in the inset of Fig. 19.

Our data suggest that stress-induced defects in the studied porous low-k dielectric are related to the degradation of the Si-O-Si network. Recent investigations indeed show that our low-k material has a Si-O based skeleton and this Si-O skeleton, rather than the pore surface, dominates the leakage current. For our material, the effect of porogen residue is minimized by the additional remote H<sub>2</sub>/He downstream plasma treatment during dielectric deposition.<sup>22</sup> The HF etching experiment performed by Verdonck *et al.* determines its chemical structure as a Si-O based skeleton inside the skeleton and methyl groups at the matrix-pore interface.<sup>36</sup> From the studies of the porosity effect, the reduced leakage current in higher porosity dielectrics, compared to the

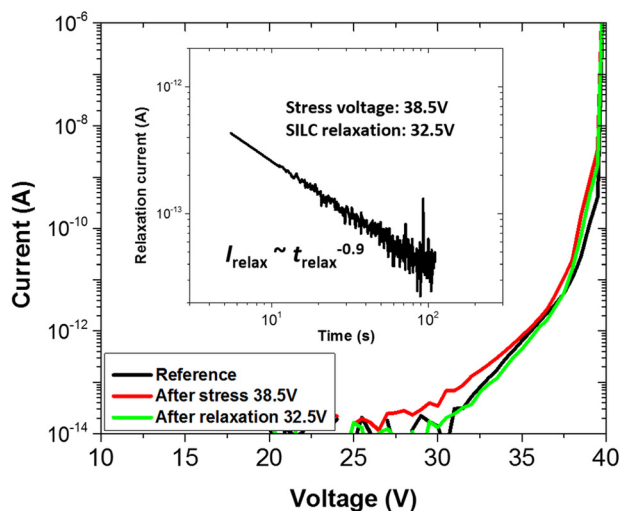


FIG. 19. Change in  $I$ - $V$  characteristics at 100 °C in the MIM capacitors with 40 nm  $\text{SiO}_2$  after being subjected to high voltage stress and high voltage stress plus low voltage relaxation. The inset shows  $I_{\text{relax}}$  behavior during low voltage storage at 100 °C.

matrix-only samples, is linked to an improved Si-O-Si skeleton.<sup>8</sup> The determined tunneling barrier height, 4 eV, in this material also indicates an  $\text{SiO}_2$  type matrix.<sup>23</sup> Finally, as shown in Fig. 20, the same leakage currents are measured on capacitors from sample S-1 with a pristine low-k dielectric and sample S-5 with a low-k dielectric after being exposed to 10 s Xe plasma. In the study of dielectric damage by vacuum ultraviolet photons reported by de Marneffe *et al.*,<sup>37</sup> carbon related groups at the pore surface, like methyl groups, are extremely sensitive to such plasma exposure. The same leakage currents again suggest that the Si-O skeleton in the dielectric determines the leakage current. As a result, stress-induced defects happening inside the Si-O-Si network of the degraded low-k material is a feasible explanation.

In  $\text{SiO}_2$ , two theories explaining defect generation processes have been proposed. One theory involves atomic hydrogen release. As shown by DiMaria and Cartier,<sup>10</sup> the leakage current in thermal  $\text{SiO}_2$  increases proportionally to the atomic hydrogen dose in a remote plasma, suggesting a strong correlation between the electrical measurements and hydrogen atom involved trap creation processes. Another possible trap creation theory is suggested by Dumin *et al.*,<sup>38</sup>

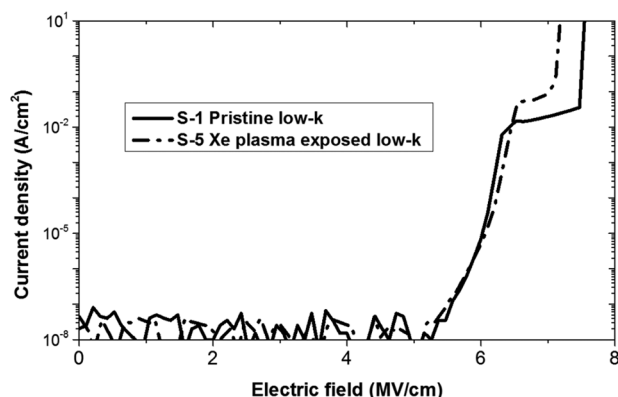


FIG. 20. Comparison of leakage current vs. electric field results measured on capacitors from sample S-1 and sample S-5 at 25 °C.

where the breakage of the Si-O bonds is proposed to be caused by impurity atoms inside the oxide, particularly hydrogen, nitrogen, argon, carbon, chlorine, and fluorine. These generated defects could then be charged positively or negatively. For our particular porous low-k material, a large negative  $V_{\text{FB}}$  shift in the  $C$ - $V$  measurement is observed in degraded samples, as shown in Fig. 18. Hydrogen atom induced donor type interface states are hypothesized to be the cause.<sup>20</sup> Thus, the degradation in our low-k material under electrical stress probably also links to the generation and movement of impurity atoms.

#### IV. CONCLUSION

We performed a detailed investigation of SILC mechanisms in an ultra-porous  $\text{SiOCH}$  low-k dielectric using dedicated planar capacitor structures. SILC increase is directly correlated with material degradation, which is dominantly driven by injected charges. Defects generated in the dielectric enhance the electron charging/discharging at the interface, leading to SILC increase. The key relation between the increase of the defect density  $N$  vs. the amount of injected charges  $Q$  follows a sub-linear form,  $N \sim Q^{0.45 \pm 0.07}$ . In highly degraded low-k dielectrics, most of these defects are found to be located between 3.4 eV and 3.6 eV below the low-k conduction band with a density level of  $1 \times 10^{18} \text{ eV}^{-1} \text{ cm}^{-3}$ . We show that these generated defects are linked to the degradation of the Si-O based skeleton in the low-k dielectric. This is because of similarities in skeleton structure and SILC characteristics when comparing our material to  $\text{SiO}_2$ . The feasibility of applying our analysis method to damascene structures, including the understanding of the impact of additional interfaces, requires further exploration.

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